What is claimed is:

1. An integrated circuit device including a first input pin through which a signal is applied to a first internal circuit and a second input pin through which a signal is applied to a second internal circuit, the integrated circuit device comprising:

a distribution unit which receives and outputs a first input signal input via the first input pin, and receives and outputs a second input signal input via the first input pin in response to a control signal;

a level fixing unit which receives the first input signal from the distribution unit and applies a signal having the same voltage level as the first input signal to a first internal circuit in response to the control signal; and

an activation unit which receives the second input signal input via the second input pin and applies the second input signal to a second internal circuit or applies the second input signal output from the distribution unit to the second internal circuit in response to the control signal.

2. The integrated circuit device of claim 1, wherein the first input signal is maintained at either a first logic level or a second logic level during a specific operation mode of the integrated circuit device.

3. The integrated circuit device of claim 1, wherein the first and second input signals are different types of signals.

4. The integrated circuit device of claim 1, wherein the control signal is generated in a specific operation mode of the integrated circuit device.

5. The integrated circuit device of claim 1, wherein the control signal is a mode register set (MRS) signal.

6. The integrated circuit device of claim 1, wherein the integrated circuit device is one of a synchronous dynamic random access memory (SDRAM), a RAMBUS DRAM, and a double data rate (DDR) DRAM.

7. An integrated circuit device including first through N-th address pins, through which first through N-th address signals are respectively applied to an

internal circuit, and a clock activation pin, through which a clock activation signal is input, the integrated circuit device comprising:

an activation unit which applies the N-th address signal input via the N-th address pin to the internal circuit or applies a predetermined address test signal to the internal circuit in response to a control signal;

a level fixing unit which receives and outputs the clock activation signal input via the clock activation pin and outputs a signal having the same voltage level as the clock activation signal in response to the control signal; and

a distribution unit which outputs the N-th address signal input via the clock activation pin as an address test signal in response to the control signal.

8. The integrated circuit device of claim 7, wherein the activation unit applies the N-th address signal input via the N-th address pin to the internal circuit when the control signal has a first logic level, and applies the address test signal to the internal circuit when the control signal has a second logic level.

9. The integrated circuit device of claim 7, wherein the level fixing unit receives and outputs a clock activation signal input via the clock activation pin when the control signal has a first logic level, and outputs a signal having the same voltage level as the clock activation signal when the control signal has a second logic level.

10. The integrated circuit device of claim 7, wherein the distribution unit is a logic NAND means performing a logic NAND operation on the control signal and the N-th address signal.

11. The integrated circuit device of claim 7, wherein the activation unit comprises:

an inverter which inverts the control signal;

a first logic NAND means which performs a logic NAND operation on an output signal of the inverter and the N-th address signal input via the N-th address pin; and

a second logic NAND means which performs a logic NAND operation on an output signal of the first logic NAND means and the address test signal.

12. The integrated circuit device of claim 7, wherein the level fixing unit comprises:

a first inverter which inverts and outputs the control signal;

a second inverter which inverts and outputs a signal input via the clock activation pin; and

a logic NAND means which performs a logic NAND operation on an output signal of the first inverter and an output signal of the second inverter.

13. The integrated circuit device of claim 7, wherein the control signal is generated to have a second logic level in a test mode of the integrated circuit device.

14. The integrated circuit device of claim 7, wherein the control signal is an MRS signal.

15. The integrated circuit device of claim 7, wherein the integrated circuit is one of a SDRAM, a Rambus DRAM, and a DDR DRAM.

16. A method of applying an N-th address signal to an internal circuit via a clock activation pin in a test mode of an integrated circuit device including first through N-th address pins, through which first through N-th address signals are respectively applied to an internal circuit, and a clock activation pin, through which a clock activation signal is input, the method comprising:

(a) determining whether the operation mode of the integrated circuit device is a test mode and applying the N-th address signal to the internal circuit via the N-th address pin if the operation mode of the integrated circuit device is not a test mode;

(b) outputting a signal having the same voltage level as the clock activation signal input via the clock activation pin in response to a predetermined control signal if the operation mode of the integrated circuit device is a test mode;

(c) outputting the N-th address signal input via the clock activation signal as an address test signal in response to the control signal; and

(d) applying the address test signal to the internal circuit in response to the control signal.

17. The method of claim 16, wherein in step (b), when the control signal has a first logic level, a clock activation signal input via the clock activation pin is received and then output, and when the control signal has a second logic level, a signal having the same voltage level as the clock activation signal is output.

18. The method of claim 16, wherein in step (d), when the control signal has a first logic level, the N-th address signal input via the N-th address pin is applied to the internal circuit, and when the control signal has a second logic level, the address test signal is applied to the internal circuit.

19. The method of claim 16, wherein the control signal is generated to have a second logic level in a test mode of the integrated circuit device.

20. The method of claim 16, wherein the control signal is an MRS signal.